

REMARKS

Claims 39-47 and 49-50 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Lee. Reconsideration is respectfully requested.

The Office Action asserts that “Lee et al discloses on figure 5 a semiconductor device comprising a substrate 31 and at least one electron mechanically polished metal layer 53 formed over said substrate 31.” (Office Action, pg. 2). Applicants respectfully disagree. Lee does not teach or suggest in any manner an “electro-mechanically polished metal layer,” as recited in claims 39, 43 and 48-51.

Lee teaches forming a diffusion barrier layer 37 in contact with a first conductive layer 39. See paragraph 38 and Fig. 5. A second conductive layer 53, used as the lower electrode of the capacitor, is formed on the first conductive film pattern 39. See paragraph 38 and Fig. 5. “The second conductive film pattern 53 used as the lower electrode is not formed by a dry etching process but by a CMP (chemical mechanical polishing) method or an etch-back method.” (Paragraph 40) (emphasis added). The cited reference teaches a conventionally formed metal layer and not Applicants’ claimed electro-mechanically polished metal layer.

The Office Action further asserts “that the term ‘electro-mechanical polished’ merely recites product by process and does not structurally distinguish the metal layer from the structure taught by Lee et al.” (Office Action, pg. 2). Applicants respectfully disagree. As explained below, even if one used the CMP method disclosed in Lee, one still would not achieve the same structure as recited in Applicants’ claims.

The literature of record demonstrates that CMP and EMP are entirely different processes resulting in significant structural differences. In “Electrochemical Planarization for Multi-Level Metallization of Microcircuitry” by Anthony F. Bernhardt et al., disclosed in Applicants’ IDS, “CMP has a tendency to dish down into the center of wide metal features, as well as causing scratching and smearing.” (Page 40, Col. 3) (emphasis added). In contrast, an electro-mechanically polished surface has structural uniformity “within two

percent,” across a wafer (Page 46, Col. 3 and FIGS. 3, 4 and 9). This is a significant structural difference from a CMP processed layer. Lee teaches a conventionally formed metal layer and not an “electro-mechanically polished metal layer” as Applicants claim.

Accordingly, Lee does not teach or suggest a semiconductor device with “at least one electro-mechanically polished metal layer,” as recited in claims 39 and 49, a semiconductor capacitor with “at least one electrode surface [that] comprises an electro-mechanically polished” surface as recited in claims 43 and 50, or a processor system with a “capacitor comprising at least one electro-mechanically polished,” layer as recited in claims 48 and 51.

For at least these reasons, dependent claims 40-42 which incorporate all of the limitations of independent claim 39, and dependent claims 44-47 which incorporate all of the limitations of claim 43, are neither anticipated by, nor rendered obvious over Lee.

Withdrawal of the § 102(b) rejection with regard to claims 39-47 and 49-50 is respectfully solicited.

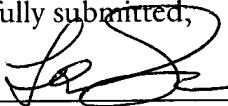
Claims 48 and 51 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Sandhu. Reconsideration is respectfully requested.

The remarks provided above with regard to the rejection of claims 39-47 and 49-50 in view of Lee are equally applicable here. Specifically, electro-mechanically polished metal layers are structurally distinct from Lee’s metal layer 53. Sandhu is relied upon as disclosing a memory device electrically coupled to a processor and adds nothing of significance to the issue of EMP layers. Accordingly, withdrawal of the § 103(a) rejection with regard to claims 48 and 51 is respectfully solicited.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By 

Thomas J. D'Amico

Registration No.: 28,371

DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 785-9700

Attorney for Applicants